Energy efficiency of quantum computers

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As quantum technologies are entering a phase of industrial development, there is an increasing interest on benchmarking their energy costs [1]. In particular, the community is starting now to explore the energy costs of quantum computers, whether they will be able to provide an energetic advantage with respect to classical computers, or be sustainable at all [2, 3, 4]. Based on the insight of several experts on different quantum computing platforms, we propose a hardware-oriented approach, and we use it to estimate the energy efficiencies of five of the best-known quantum computing platforms: superconducting qubits, spin qubits, trapped ions, neutral atoms, and photonic quantum computers. For each of them, we analyze significant architectural variations to showcase the versatility of our framework and how it can guide design or policy making decisions.

Our work stems from the observation that quantum computers have a stable power consumption independently of the algorithm that they are executing, and even if they are not performing operations. We thus benchmark their energy consumption based on the amount of computations that they can run for a given energy expenditure in a given time. We introduce the energy efficiency of quantum computers, that quantifies how many algorithms can be executed per energy unit:

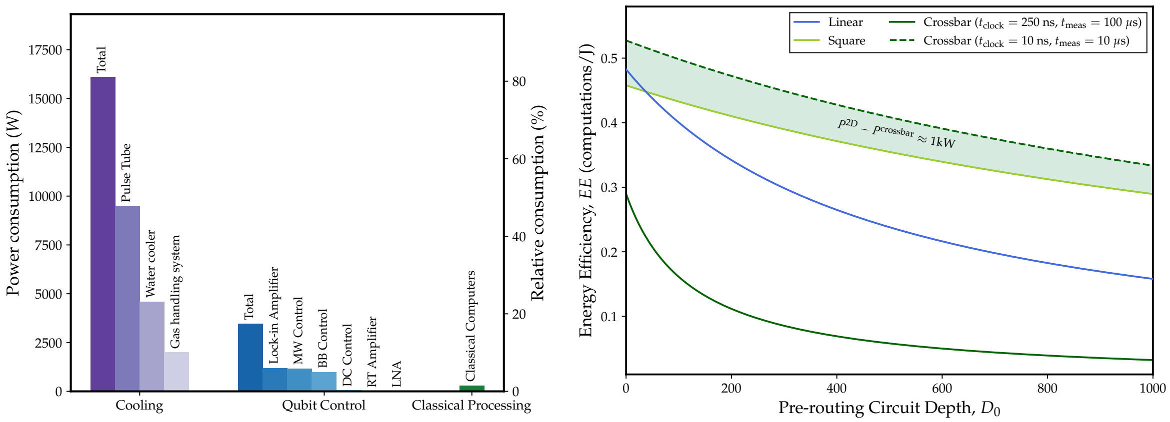
$$EE^{\pi}_{\mathcal{A}} = \frac{\text{\# Algorithms performed in time t}}{\text{Energy consumed in time t}} = \frac{N^{\pi}_{\mathcal{A}}(t)}{E^{\pi}(t)} = \frac{1}{t_{\mathcal{A}} \cdot P^{\pi}}, \tag{1}$$

where $N^{\pi}_{\mathcal{A}}(t)$ is the number of executions of an algorithm $\mathcal{A}$ performed in time t by a computer π, $t_{\mathcal{A}}$ is the time to execute the algorithm, and P^{π} is the total consumption of the hardware present in the device.

We estimate the overall power consumption of a quantum computer as the sum of the list of hardware components, assuming that this consumption is constant, independently of whether the device is running an algorithm or not. This assumption is faithful to existing quantum computers, that experiment negligible peaks of power consumption when executing operations, accordingly to our observations. For each of the five main platforms, we provide an example of a device, based on real current implementations and the literature, and break down their power consumption, to identify the main consuming elements. Panel (a) of Figure 1 displays the power consumption of all the hardware components in a spin-qubits computer.

On the other hand, we develop a detailed model to estimate the running time of algorithms. We identify the most time-consuming operations, *e.g.* the application of 2-qubit gates or the shuttling of atoms. In addition, we consider several compilation constrains that have a deep impact on the energy efficiency of quantum computers, since they determine the depth of the circuits implementing algorithms. The interplay between hardware components, computing time, and circuit compilation, results in energy efficiency tradeoffs between architectures.

Based on this information, we estimate the energy efficiency of computers running algorithms for a wide range of number of shots and algorithm depths. By choosing algorithm depth and number of shots as variables in our model, we avoid having to select a specific task to benchmark quantum computers. Finally, we are able to use our framework to compare different architectures that are currently relevant for each of the quantum computing platforms considered in our work. As an example, Panel (b) of Figure 1 displays the energy efficiency of four spin-qubits architectures, depending on their connectivity and wire multiplexing. While platforms are in different stages of maturity and can be specialized in certain tasks, our works allows to benchmark their energy consumption with a unified framework.



(a) (b)

Figure 1: Example of results from our work. Panel (a) shows the power consumption breakdown of a spin-qubit quantum computer. Panel (b) shows a comparison between the energy efficiencies of different spin-qubits architectures, depending on the depth of the circuit before adding SWAP gates to solve the connectivity constrains. The computer shown in Panel (a) has a linear connectivity graph, represented with a blue curve in Panel (b).

References

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